Amendments to the specification:

On page 1, after the title, please add the following:

CROSS-REFERENCE TO RELATED APPLICATION(S)

This application is a divisional of copending application U.S. Serial No. 09/848,137, filed on May 3, 2001.

On page 1, line 17 to page 2, line 3, please amend the paragraph as follows:

A few of the patents related to WLCSP technologies are listed in the following:

- U.S. Patent 6,103,552 "WAFER SCALE ~~PAKCAGING~~ PACKAGING SCHEME";
- U.S. Patent 6,011,314 "REDISTRIBUTION LAYER AND UNDER BUMP ~~MATEERIAL STRUCUTRE~~MATERIAL STRUCTURE FOR CONVERTING PERIPHERY CONDUCTIVE PADS TO AN ARRAY OF SOLDER BUMPS"[[.]];
- U.S. Patent 5,902,686 "METHODS FOR FORMING AN ~~INTERMEALLIC~~ INTERMETALLIC REGION BETWEEN A SOLDER BUMP AND AN UNDER BUMP METALLURGY LAYER AND RELATED ~~STRUCUTRES~~STRUCTURES";
- U.S. Patent 5,851,911 "MASK REPATTERN PROCESS"; and
- U.S. Patent 5,450,283 "THERMALLY ENHANCED SEMICONDUCTOR DEVICE HAVING ~~EPOXED~~ EXPOSED BACKSIDE AND METHOD FOR MAKING THE SAME".

Please amend the paragraph on page 3, lines 10-12 as follows:

It is still another objective of this invention to provide a new WLCSP technology that can prevent the packaged chip from being cracked or chipped by external force during ~~handing~~ handling or transportation.

Please amend the paragraph on page 5, lines 15-19 as follows:

Referring further to FIG. 3, in the next step, a back-side lapping process is performed to grind away a back-side portion 10c (see FIG. 2) of the semiconductor wafer 10. This allows the semiconductor wafer 10, whose raw thickness is typically from 25 mil to 30 mil, to be thinned down to about from 6 mil to 10 mil in thickness. The thinned wafer 10 allows the final package size to be made more compact in thickness.